



Original Research Paper

# A COMPREHENSIVE REVIEW ON FAULT TOLERANCES, ROUTING TECHNIQUES AND ENERGY EFFICIENCY IN NETWORK ON CHIP ARCHITECTURES

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## ABSTRACT

All our modern processors are all belong to multicore processors. A new category of processors, where multiple processing units are housed on a single chip. According to Jordan Moore predicted that the number of transistors inside a chip is going to double every eighteen months. The advances in VLSI Innovations have brought out the Network-on-Chip (NoC) as an essential solution to handle the network communication issues in complex multi-core systems. Meanwhile, NoCs is a flexible and efficient solution for data communication within multi-core microprocessors as the complexity of semiconductor technology grows.

This survey paper makes a comprehensive analysis of the innovation, problem and application conduct that has been made by NoCs in multi-core systems. The paper starts with a background from where the focus is shifted to modern multi-core processors along with the significance of NoCs in improving the inter-core connectivity. For one, it makes a comprehensive survey of NoC design parameters or strategies for topologies, routing algorithms, and protocols and unveils the extent of the influence of NoC designs on the performance and scalability effect of the NoC.

It also summarises the key limitations of NoC implementation that includes power management, reliability, and congestion control. Other important matters concerning the use and utilization of bandwidth and the issue of latency is also addressed as well provided us to squeeze in more number of transistors inside a chip. Package density of transistors has increased very high. More number of transistors inside chip permits us to include more number of functional units like processors, memory, control unit etc inside a chip. In the era of "Internet of Things and IOT and Artificial

Intelligence and there is a requirement to collect and process huge data, and many of the applications are in real time, which demands high computation power, a massive parallel computers.. To address these challenges, the paper offers solutions as follows, which are the new design strategies, energy efficient and fault tolerant schemes which endeavour to improve on the overall performance of NoC as a design topology in large scale multiple core processing.

As is presented, potential uses of NoCs are identified in a number of novel application areas such as high-performance computing, IoT and artificial intelligence, demonstrating that NoC architectures maintain and enhance their relevance. Last, the paper discusses future work, and presents more details on why NoCs have to be adaptive, self-organizing structures, which will be sufficient for supporting multi-core systems of the next generation. NoC is a promising technology for multi-core systems and this survey serves as a good starting point for researchers, engineers and technologists in this field.

**Keywords:** *Network-on-Chip, multi-core systems, routing algorithms, energy efficiency, fault tolerance*

## INTRODUCTION

NOC has become a promising architectural solution, which appeared a few years ago to solve communication problems in multi-core and many-core processors. Due to these issues, as the requirement for greater computational capability in the processing system is on the rise, the advancement of intelligent computing and network technologies has created opportunities for improving the efficiency, scalability, and reliability of modern computational systems [1]. Conventional bus-based communication has numerous disadvantages such as limited bandwidth, power dissipation, and the problem of

scalability. NOCs provide a promising solution by providing a low overhead mechanism to effectively and cheaply communicate between different processing elements on a chip to improve the design of today's complex chips. The integration of intelligent computing, networked systems, edge computing, and energy-efficient technologies has become increasingly important for developing efficient and reliable modern computational architectures [2]. From this survey paper, the challenges in developing the NOC are highlighted specifically the multi-cores, fault tolerance, Power consumption, and memory.

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## BACKGROUND AND LITERATURE REVIEW

Semiconductor technology has undergone development due to the demand for more computation. With increasing levels of sophistication in the production of integrated circuits (ICs) the density of transistors continues to rise, resulting in multi-and many-core processors. Each of these processors is meant to perform several operations at once and deliver significantly higher performance than single-core systems. However, with the development of single-core and Multi-core processors, there is a new problem of how best to interconnect these cores for efficient computation (Reza, 2023) [3]. The existing bus-based communication has been seen to be unsuitable for large-scale systems that have high integrity requirements. As a result of this kind of interconnection, modern SoC designs have seen a shift towards the use of Network-on-Chip (NOC) architectures which can accommodate multi-core processors since they are more scalable, efficient, and also fault tolerant.

### Literature Review

NOC as a technology has been explored widely in the literature and numerous advancements in the area have been pioneered in terms of architecture, design methodologies, reliability, power management, and memory hierarchies. In the early NOC development, many of the research emphases were put on reasonable topology designs and routing protocols (Sharma et al., 2021) [7]. Recent works in this area reflect this with power optimization, resiliency to faults, and memory efficiency all while keeping high performance. The next several sections present a review of the literature on the main areas of research in NOC technology.

### 1. Topologies and Architectures of NOC

The most crucial element of decision in any NOC system is the topology that underlines the network. Different topologies have been conceptually and physically deployed and each has strengths and weaknesses. Popular NOC architectures are mesh, torus, tree, and ring. Thus, topologies differ one from the other regarding their scalability, communication delay, and routing problems (Zhang et al., 2024) [8].

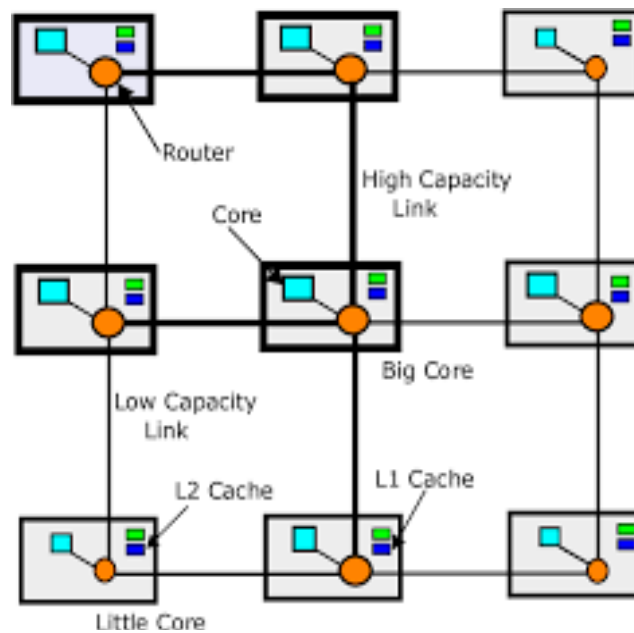


**Figure 1:** Multi-Core NOC Architecture

This is another reason why the mesh topology is one of the most used NOC architectures because of its simplicity and expansion capabilities. A mesh network is established when nodes (commonly routers) are arranged in a way that they are directly connected forming a grid-like pattern (Olusegun et al., 2024) [9]. This topology enables any two nodes can communicate with each other even though the distance between them rises as more cores are added. The torus topology which is an extension of the mesh interconnects the edges of the mesh forming a ring cycle and thus has longer average reachability and scalability than the mesh.

### 2. Routing Algorithms

Routing forms one of the most important structural concepts in NOC, because it is through routing that data is managed within the network. A good routing algorithm would mean that signaling delays are reduced, power wastage is prevented and the use of the available resources is optimized. Routing algorithms are generally classified into two categories: deterministic and adaptive (Poovendran, 2023) [12].

**Table 1: Routing Algorithm Classification**

| Algo-rithm Type         | Exam-ples                       | Char-acteristics              | Ad-vantages                            | Dis-ad-vantages                             | Ref-erences                      |
|-------------------------|---------------------------------|-------------------------------|----------------------------------------|---------------------------------------------|----------------------------------|
| De-terminis-tic         | XY Routing, Dimen-sion-Or-dered | Fixed paths based on layout   | Sim-ple, low overhead                  | Lim-ited flexi-bility, traf-fic con-gestion | (Kon-doth et al., 2023) [13]     |
| Adap-tive               | Worm-hole, Buff-erless          | Path changes with con-ditions | High flexibil-ity, con-gestion control | Com-plex im-plementa-tion                   | (Nab-avinejad et al., 2020) [14] |
| Rein-forcement Learning | RL-Based Routing                | Learns from traf-fic patterns | Pro-active, adaptive, energy-efficient | Train-ing com-plexity                       | (Reza and Le, 2021) [59]         |

**Table 2: Comparison of NOC Topologies**

| Topology          | Struc-ture                                | Ad-vantages                         | Disad-vantages                    | Refer-ences                      |
|-------------------|-------------------------------------------|-------------------------------------|-----------------------------------|----------------------------------|
| Mesh              | Grid-like ar-rangement of nodes           | Simple, scalable, easy to ex-pand   | In-creased de-lay with more cores | (Olusegun et al., 2024) [9]      |
| Torus             | Mesh with con-nected edges                | Better scalability than mesh        | Com-plex wiring                   | (Olusegun et al., 2024) [9]      |
| Tree              | Hier-archical clusters of nodes           | Efficient local communica-tion      | Root congestion risk              | (Muhsen et al., 2024) [10]       |
| Ring              | End-to-end connected nodes forming a loop | Simple, cost-effec-tive             | High la-tency, mul-tiple hops     | (Muhsen et al., 2024) [10]       |
| Adap-tive/Dynamic | Struc-ture changes with sys-tem load      | Self-ad-justs, re-duced con-gestion | Com-plex to im-plement            | (Bal-amurugan et al., 2022) [11] |

### 3. Fault Tolerance in NOCs

With size, it is expected that the rate of component failures also increases in multi-core systems. Reliability and survivability in NOCs have been identified as critical study areas given the need to manage fault incidents in

communication networks (Al-Alousi, 2024) [15]. Heterogeneous solutions have been suggested to provide fault detection and recovery mechanisms that will keep the system running even when the components of the network, which may act erroneously, are still present.

**Table 3: Fault Tolerance and Power Efficiency Techniques in NOCs**

| Technique                        | Description                                       | Benefits                              | Challenges                        | References                       |
|----------------------------------|---------------------------------------------------|---------------------------------------|-----------------------------------|----------------------------------|
| Redun-dant Paths                 | Multi-ple paths for data transfer                 | Fault tolerance, improved reliability | In-creased area and complexity    | (Al- Alousi, 2024) [15]          |
| Error Correction Codes           | Data encoding for error detection and correc-tion | Data re-liability, re-duced fail-ures | Over-head due to encoding process | (Gupta et al., 2024) [16]        |
| Power Gat-ing/Clock Gating       | Switch-ing off in-active com-ponents              | Re-duced power consumption            | Perfor-mance overhead             | (Das et al., 2024) [17]          |
| Dy-namic Volt-age Scaling (DVFS) | Adjust-ing voltage based on load                  | Energy efficiency                     | Com-plex power manage-ment        | (Das et al., 2024) [17]          |
| Cache Coherence Protocols        | En-sures con-sistency in shared memory            | Correct memory ac-cess                | In-creased memory traffic         | (Ve- layudham et al., 2021) [18] |

### Reinforcement Learning for Congestion Control

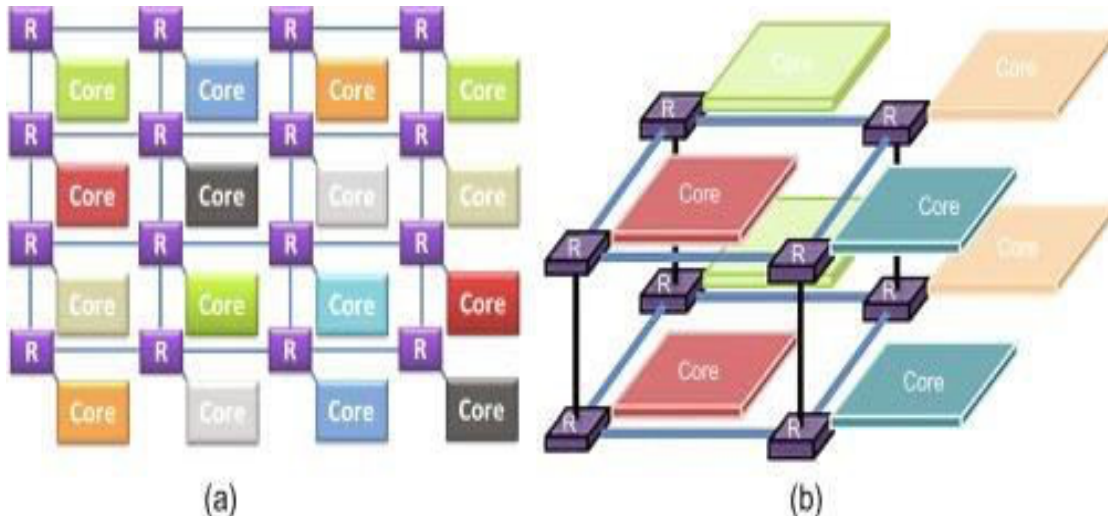
The reinforcement learning (RL) enabled routing solves congestion management in Network on-chip (NoC)

systems by providing a proactive approach to increase system performance and energy efficiency

#### 4. Power Efficiency in NOCs

Power consumption is one of NOC's major challenges in multi-core systems that grow with the number of cores. Battery charging and discharging is an important function

because it maintains heat and charge of the system as well as energy consumption. This paper has reviewed several strategies for improving power in NOCs.



#### 5. Memory Management in NOCs

The role of memory management must also be optimized within NOC-based systems because processors require rapid access to significant quantities of information from

shared memory or distributed memory domains. Getting memory access right and controlling latency proves to be more complicated due to escalating numbers of cores and more complex memory hierarchies.

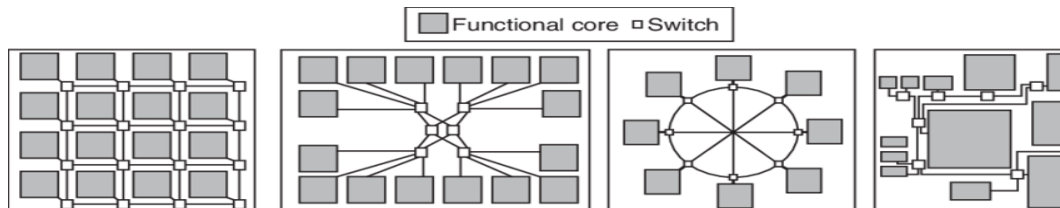


**Figure 6:** Interconnect Architecture of NOC Problem Formulation and Challenges

#### Problem Formulation

Today's and future applications of computer systems have been made easier by the development of semiconductor technologies especially in multi-core processors. With the increase in the number of cores within a chip, it becomes increasingly important to develop a communication network that masters escalating data flow between these cores

#### Scalability Low Latency

**High Throughput Fault Tolerance Power Efficiency Cost Efficiency**

#### Quality of Service (QoS)

#### Issues of the NOC-Based Multi-Core Systems

1. Scalability and Network Congestion.
2. Latency and Communication Delay
3. Power Consumption and Energy Efficiency
4. Dependability and Redundancy

#### 5. Memory Management and Cache Coherence

#### 6. Quality of Service (QoS)

**Proposed Solutions:** Due to a variety of obstacles being faced by multi-core systems based on NOC, multiple innovative methods have been developed. All the mentioned solutions are intended for achieving high system data throughput with minimum response times, minimum power consumption, system scalability, fault tolerance of a system, quality of service (QoS) demands, etc. Below are some of the most promising approaches to solving these challenges:

#### IV. Evaluation Metrics and Model Performance

#### 1. Scalable Network Topologies Mesh and Torus Topologies Fat-Tree and Clos Networks

#### Hierarchical and Hybrid

**Low Power and Energy Sensitive Methods Dynamic Voltage and Frequency Scaling (DVFS) Power Gating**

**Low-Power Components Energy-Aware Routing**

#### 4. Fault Tolerance and Reliability Solutions Future Trends and Applications: Redundant Paths and Fault Recovery Error Detection and Correction:

NoC Fault Simulation and Testing:

#### 5. Memory Management and Cache Coherence Solutions Cache Coherence Protocols:

Non-Uniform Memory Access (NUMA)

#### 6. Quality of Service (QoS) Management

.Traffic Shaping and Prioritization:

Bandwidth Reservation. Latency-Aware Routing.

#### Potential Applications and Future Work

Multi-core, Network-on-Chip (NoC) based systems are the building blocks of modern computing designs and proposed to yaklaş the paradigms of high performance and low energy communication between cores in multiprocessor systems on a chip. With the rising necessity for superior and multi-functioned systems

##### 1. HPC stands for High-Performance Computing

##### 2. Structuring of Data Center and Cloud Computing

##### 3. Internet of Things (IoT)

##### 4. Automotive and Automobile Cars

##### 5. Healthcare and Medical Systems/DevicesNoCs

#### V. CONCLUSION

It is necessary to argue that multi-core processors' constant evolution and the development of innovative NoC systems have become a breakthrough point in the development of contemporary computing platforms. As a response to the communication issues that result from multi-core technologies

#### VI. REFERENCES

- [1] Phalguni, Malik, A. S., & Chand, G. (2024). The Future of Healthcare in India: Artificial Intelligence and Machine Learning-Driven Predictive Analysis for Quality Healthcare Delivery in Healthcare Sector. *Bulletin of Pure and Applied Sciences-Zoology*, 43A(2S).
- [2] Mohammad, S. I., & Vasudevan, A. (2026). IoT-Enabled Smart Irrigation System for Efficient Water Management in Agriculture. *Journal of Experimental Biology and Agricultural Sciences*, 14(3), pp. 29–34. Retrieved from <https://jebas.org/ojs/index.php/jebas/article/view/3799>

- [3] Reza, M.F., 2023. Machine learning enabled solutions for design and optimization challenges in networks-on-chip based multi/many-core architectures. *ACM Journal on Emerging Technologies in Computing Systems*, 19(3), pp.1-26.
- [4] Saleem, S., Hussain, F., Amin, W., Ahmed, R., Zikria, Y.B., Ishmanov, F. and Yu, H., 2023. A Survey on Dynamic Application Mapping Approaches for Real-Time Network-on-Chip-Based Platforms. *IEEE Access*, 11, pp.122694-122721.
- [5] Asadi, Y., 2024. A comprehensive study and holistic review of empowering network-on-chip application mapping through machine learning techniques. *Discover Electronics*, 1(1), pp.1-25.
- [6] Husin, N.A., Zolkepli, M.B., Manshor, N., Al-Hchaimi, A.A.J. and Albahri, A.S., 2024. Routing Techniques in network-on-chip based multiprocessor-system-on-chip for IOT: a systematic review. *Iraqi Journal For Computer Science and Mathematics*, 5(1), pp.181-204.
- [7] Sharma, G., Bousdras, G., Ellinidou, S., Markowitch, O., Dricot, J.M. and Milojevic, D., 2021. Exploring the security landscape: NoC-based MPSoC to Cloud-of-Chips. *Microprocessors and Microsystems*, 84, p.103963.
- [8] Zhang, X., Dong, D., Li, C., Wang, S. and Xiao, L., 2024. A survey of machine learning for Network-on-Chips. *Journal of Parallel and Distributed Computing*, 186, p.104778.
- [9] Olusegun, J., Andrew, D., Alex, F. and Frank, E., 2024. Review of Energy-Efficient NoC Router Design Techniques.
- [10] Muhsen, Y.R., Husin, N.A., Zolkepli, M.B., Manshor, N., Al-Hchaimi, A.A.J. and Albahri, A.S., Routing Techniques in Network-On-Chip Based Multiprocessor-System-on-Chip for IOT: A Systematic.
- [11] Balamurugan, K., Umamaheswaran, S., Mamo, T., Nagarajan, S. and Namamula, L.R., 2022. Roadmap for machine learning based network-on-chip (M/L NoC) technology and its analysis for researchers. *Journal of Physics Communications*, 6(2), p.022001.
- [12] Poovendran, R., 2023. Design a wireless network on chip (NoC) architecture for multi-core platforms with optimized topology.